What is claimed is:

1. A method for operating a flash memory device that is constituted by arraying silicon-oxide-nitride-oxide-semiconductor (SONOS) memory cells including a drain and a source formed in a substrate, a channel formed between the drain and the source, a gate formed over the channel, and a multi-layered dielectric layer of an oxide layer, a nitride layer, and an oxide layer formed between the gate and the substrate in the NOR form, the method comprising:

applying voltages to one selected from the SONOS memory cells and programming the selected SONOS memory cell so that hot electrons are injected into at least one of either the interface between the oxide layer and the nitride layer or into the nitride layer from the channel and trapped in at least one of either the interface between the oxide layer and the nitride layer or in the nitride layer to increase a threshold voltage; and

applying a positive voltage to the substrate, at least one of either a ground voltage or a negative voltage to the gate and floating at least one of either the source or the drain to reduce the threshold voltage to perform at least one of either removing trapped electrons using Fowler-Nordheim tunneling or erasing the trapped electrons by injecting hot holes created between one of either the source and the substrate or between the drain and the substrate under the voltage condition into the multi-layered dielectric layer.

2. The method of claim 1, wherein when the selected SONOS cell is programmed, a voltage is applied to the selected SONOS cell in a condition that a voltage within a range of 8V – 12V is applied to the gate of the selected SONOS cell, a voltage within a range of 3V – 6V is applied to the drain, and the source is ground.

3. The method of claim 2, wherein the condition further comprises at least one of either grounding the substrate or applying a negative voltage to the substrate.

4. The method of claim 1, wherein when erasing the trapped electrons, the gate of the selected SONOS memory cell is ground and a voltage within a range of 13V – 18V is applied to the substrate.

5. The method of claim 1, wherein when erasing the trapped electrons, a voltage of about –8V is applied to the gate of the selected SONOS memory cell and a voltage of about 6V is applied to the substrate.

6. A method for operating a flash memory cell that is constituted by arraying silicon-oxide-nitride-oxide-semiconductor (SONOS) memory cells including a drain and a source formed in a substrate, a channel formed between the drain and the source, a gate formed over the channel, and a multi-layered dielectric layer of an oxide layer, a nitride layer, and an oxide layer formed between the gate and the substrate in the NOR form, wherein drains of the SONOS memory cells are electrically connected to a bit line, gates of the SONOS memory cells are electrically connected to a word line crossing the bit line, sources of the SONOS memory cells connected to the word line are connected to a common source line, the method comprising:

applying a voltage to one selected from the SONOS memory cells and programming the selected SONOS memory cell so that hot electrons are injected into at least one of either the interface between the oxide layer and the nitride layer or into the nitride layer from the channel and trapped in at least one of either the interface between the oxide layer and the nitride layer or in the nitride layer to increase a threshold voltage; and

applying a positive voltage to the substrate, at least one of either a ground voltage or a negative voltage to the gate and floating at least one of either the source or the bit line to reduce the threshold voltage to perform at least one of either removing the trapped electrons from the interface between the oxide layer and the nitride layer or the nitride layer using Fowler-Nordheim tunneling or erasing the trapped electrons by injecting hot holes created between at least one of either the source and the substrate or between the drain and the substrate under the voltage condition into the multi-layered dielectric layer.

7. The method of claim 6, wherein when programming the selected SONOS memory cell, the voltage is applied to the selected SONOS memory cell in a condition that a word line is selected and a voltage within a range of 8V – 12V is applied to the selected word line, a bit line is selected and a voltage within a range of 3V – 6V is applied to the selected bit line, and the common source line is ground.

8. The method of claim 7, wherein the condition further comprises at least one of either grounding the substrate or applying a negative voltage to the substrate.

9. The method of claim 6, wherein when erasing the trapped electrons, the word line is ground and a voltage within a range of 13V – 18V is applied to the substrate.

10. The method of claim 6, wherein when erasing the trapped electrons, a voltage of about –8V is applied to the selected word line connected to the selected SONOS memory cell.

11. The method of claim 1, wherein at least one of either removing trapped electrons using Fowler-Nordheim tunneling or erasing the trapped electrons by injecting hot holes created between one of either the source and the substrate or between the drain and the substrate under the voltage condition into the multi-layered dielectric layer further comprises both Fowler-Nordheim tunneling and by injecting hot holes.

12. The method of claim 6, wherein at least one of either removing trapped electrons using Fowler-Nordheim tunneling or erasing the trapped electrons by injecting hot holes created between one of either the source and the substrate or between the drain and the substrate under the voltage condition into the multi-layered dielectric layer further comprises both Fowler-Nordheim tunneling and by injecting hot holes.